



# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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First Named Inventor	Rajski
Art Unit	Unknown
Examiner Name	Unknown

## U.S. PATENT DOCUMENTS

NOTE: If this application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
rw		4,511,967	April 16, 1985	Witalka et al.
		4,947,395	August 7, 1990	Bullinger et al.
		5,226,149	July 6, 1993	Yoshida et al.
		5,239,262	August 24, 1993	Grutzner et al.
		5,369,646	November 29, 1994	Shikatani
		5,416,783	May 16, 1995	Broseghini et al.
		5,590,354	December 31, 1996	Klapproth et al.
		5,617,531	April 1, 1997	Crouch et al.
		5,724,603	March 3, 1998	Nishiguchi
		5,790,561	August 4, 1998	Borden et al.

## OTHER DOCUMENTS

Examiner's Initials*	Cite No. (optional)	
rw		Edirisooriya, et al., "Minimizing Testing Time in Scan Path Architecture," IEEE Circuits and Systems, 1992 Midwest Symposium, pages 1205-1207.
		Zacharia, et al., "Decompression of Test Data Using Variable-Length Seed LFSRs," Microelectronics and Computer Systems Laboratory, McGill University, Montreal, Canada.
		Adham, et al., "Arithmetic Built-in Self Test for Digital Signal Processing Architectures," in Proceedings of the IEEE 1995 Custom Integrated Circuits Conference, May 1-4, pages 29.6.0 - 29.6.4.

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\* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

